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Techniques for the Improvement in the Transconductance of a Bulk Driven Amplifier

Kshitij Shant , Rita Mahajan
(Dept. of Electronics and Communication, PEC University of Technology, Chandigarh, India)
(Dept. of Electronics and Communication, PEC University of Technology, Chandigarh, India)

ABSTRACT
This paper proposed methods for the improvement of transconductance in the bulk driven operation amplifier. Here we are using four technologies for the enhancement of transconductance. First modifies the transconductance with the help of active load; second uses a differential pair for the modification transconductance, while third is the proposed bulk-driven input stages with modified low voltage cascode biasing scheme whereas last is the bulk driven input stage with enhanced effective transconductance. All the above methods are used to enhance the transconductance which gets decreased.
Keywords - transconductance, bulk-driven, cascade biasing.

I. INTRODUCTION

This is an era of miniaturization; everybody wants every device to be portable and can operate for many hours. In biomedical application there are so many requirements of such devices which take very low power and can withstand for large amount time. As we want to decrease the voltage supply to minimum, there is much restriction in decreasing the threshold voltage. It can only decrease up to certain level. To avoid this restriction of threshold voltage, a bulk driven technology is employed without changing the structure of MOSFET. But the problem with the bulk driven technology is that it reduces the transconductance of an operational amplifier.

Generally, the supply voltage required by an amplifier should at least equals to maximum threshold voltage value of either of the NMOS or the PMOS transistor plus signal swing [1]. The reason why the threshold voltage is not decreased as decrement in the supply voltage over the years is mostly because it provides good noise immunity.

There are numbers of voltage driven techniques which have been developed without using expansive low V_T transistor such as design utilizing bulk driven MOSFETs [1] or floating gate MOSFETs [2], sub threshold design [3] and level shifting techniques [4]-[5], etc. All the above mentioned methods have it various advantages in different applications. Out of them, the most extensively exploited technique is the bulk driven technique.

The operation of bulk driven MOSFETs is much similar to the operation of JFETs. By connecting the gate terminal with sufficient fixed voltage, the inversion layer is formed beneath the gate of the transistor. The inversion layer beneath the gate of a MOSFET is the conduction channel of the JFET. The bulk potential of a MOSFET decides the thickness beneath the drain, source and the inversion layer. The thicknesses of depletion layer gets changes by varying bulk-source voltage and also modulate the flow of drain current. Hence with very small dc value of the bulk-source potential, the channel current can be modulated which is very useful for low voltage applications.

The performance of gate-driven MOSFET is same as the performance of bulk-driven MOSFET. The only repudiations are related to the size of bulk which can be corrected by using layout techniques. In most of the application where $V_{SB} > 0.3V$, the current flow in the bulk terminal is in picoampere which is insignificant. The noise in gate-driven MOSFET is approximately equal to the noise in bulk-driven MOSFET. Due to the resistance of bulk there is a slight increase in thermal noise. Resistance of bulk can be modify by normal layout practice.

Organization:

This paper introduces and discussed the methods for the improvement of transconductance in bulk driven operational amplifier and is divided in four main sections. In first section reader is introduced to conventional bulk and gate driven differential pair. Second section will explain and discuss the methods to improve transconductance in bulk-driven operational amplifier. Third section we will discuss about the various noise in the all four mentioned techinques. Fourth section concludes our paper.

II. CONVENTIONAL BULK AND GATE DRIVEN DIFFRENTIAL PAIR

As bulk-driven transistors only PMOS devices can be used for a standard n-well CMOS process. In Fig.1 (a) bulk-driven PMOS in a differential pair is shown. To ensure that both the devices operates in

saturation region, transistors MI_{A-B} biased by negative power supply. The experiment performed by [1] provides that the input common mode voltage (V_{CM}), without turning on the bulk-to-source junction diode can swing almost rail to rail. In Fig. 1(b) the high threshold voltage ($V_{T)}$ limited V_{CM} range due to gate-driven differential pair. In fig. 1T(b) maximum V_{CM} is defined by,

$$V_{max,\,CM} = V_{DD} - V_{DS,\,sat\,(M\,TAIL)} - V_T \qquad (1)$$

Where $V_{DS,\,sat\,(M\,TAIL)}$ is onset saturation voltage. The important issue related to bulk-driven differential pairs is its small bulk transconductance (g_{mb}) as compared to transconductance (g_m) . The ratio ή of g_m to g_{mb} is expressed as,

$$\eta = \frac{g_{mb}}{g_m} \qquad (2)$$

Depending upon the bulk-to-source voltage V_{BS} , the ratio ή only ranges from 0.2 to 0.4 only if the bulk-to-source junction is not forward biased. Another drawback of bulk-driven in Fig. 1(a) is that the gate terminal will pick up the noise generated by the negative power supply also power supply rejection is poor as compare to the gate-driven circuit in fig. 1(b).

Whenever in the designing of low voltage amplifier bulk driven approach is used then there is always a limitation in the transconductance which become 3 to 5 times smaller than earlier. There various methods that are used to improve the transconductance of a bulk-driven amplifiers.

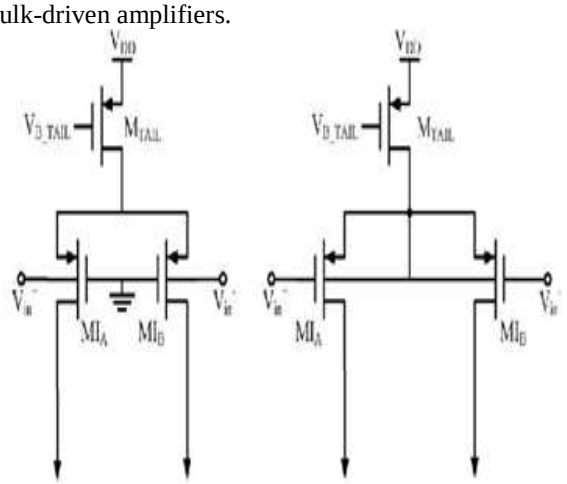

Fig.1. (a) Conventional bulk driven PMOS differential pair; (b) Simple gate driven PMOS differential pair.

III. METHODS TO IMPROVE TRANSCONDUCTANCE OF A BULK-DRIVEN AMPLIFIER

The main objective of this paper is to obtain similar value of transconductance in bulk-driven transistor as in gate-driven

1. Enhancement of transconductance by active load

The primary objective of this technique is to decrease the conductance to obtain an effective transconductance. Figure 2 shows the circuit for the enhancement of transconductance by active load [6], [7]. To mirror the current flowing from the input devices (MI) to the output branch, a diode connected transistors (MLN) are used. A partial positive feedback shown in figure 2 is been implemented by transistor MLP [8]. Due the effect of these devices the conductance at node A and B gets decreases and thus the effective input transconductance ($g_{m,eff}$) equals to

$$g_{m,eff} = g_{mb,MI} = \frac{1}{1 - \dfrac{g_{m,MLP}}{g_{m,MLN}}} = g_{mb,MI}\,\frac{1}{1-\eta_1} \qquad (3)$$

where $g_{m,MI}$ is the gate transconductance whereas $g_{mb,MI}$ is the bulk transconductance of generic transistor MI. To avoid the overall feedback to become positive, $g_{m,MLP}$ should be smaller $g_{m,MLN.}$

The circuit will be very prone to instability whenever η_1 is close to unity. For the enhancement of transconductance, the term $1/(1-\eta_1)$ is adjusted by appropriate design choices to get desired value of transconductance which is greater than unity. Also the enhancement of transconductance can also be adjusted by selecting the size of W/L ratio of both the transistors MLP and MLN. In CMOS technology, with a very high accuracy the desired value of the transconductance can be achieved very easily. Since an n-well technology is considered therefore PMOS implementation is chosen for differential pair.

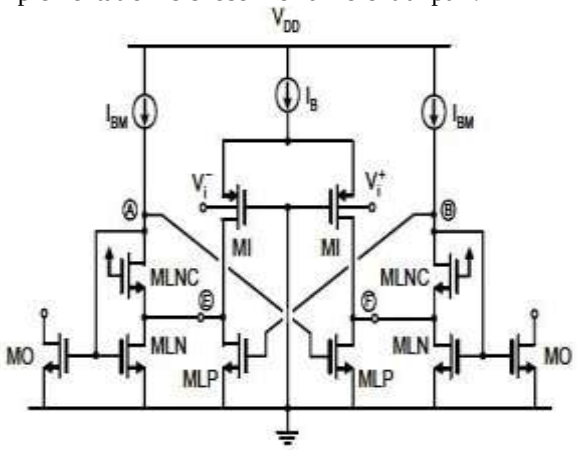

Fig. 2 Enhancement of transconductance by active load

2. Enhancement of transconductance by input differential pair

Enhancement of transconductance by input differential pair has been shown in the figure 3.

Transistor MI each biased with the current $I_B/2$ represents the input device. Signal V_{i+} and V_{i-} are applied to the bulk terminal of transistors MI. A partial positive feedback action is performed by transistor MP. To speed up the transient response, very small current I_{BA} are included in the circuit. By this, the effective impedance of the transistor at the source terminal gets modified. The effective transconductance $g_{m,eff}$ of the circuit can be expressed as

$$g_{m.eff} = g_{mb,MI}\frac{\dfrac{g_{m,MP}}{g_{m,MI}+g_{mb,MI}}}{1-\dfrac{g_{m,MP}}{g_{m,MI}+g_{mb,MI}}} = g_{mb,MI}\frac{\eta_2}{1-\eta_2} \quad (4)$$

where $\acute{\eta}_2 = g_{m,MP}/(g_{m,MI} + g_{mb,MI})$. Whenever the value of $\acute{\eta}_2 > 0.5$ then only the value of $g_{m,eff}$ gets increased. The sizes of transistor MP and MI is selected so as to adjust $\acute{\eta}_2/(1-\acute{\eta}_2)$ to desire value. If when MP and MI are made equal, transconductance factor becomes equal to $g_{m,MI} / g_{mb,MI}$. Therefore the $g_{m,eff}$ of input stage becomes equal to $g_{m,MI}$. In this approach, due to partial positive feedback the conductance reduction causes sign inversion. It should be checked to determine the polarity of input terminals. The transistor MLN, MLNC, and MO shown in figure 2 are also used to form a current mirror circuit which is necessary when we are using this technique.

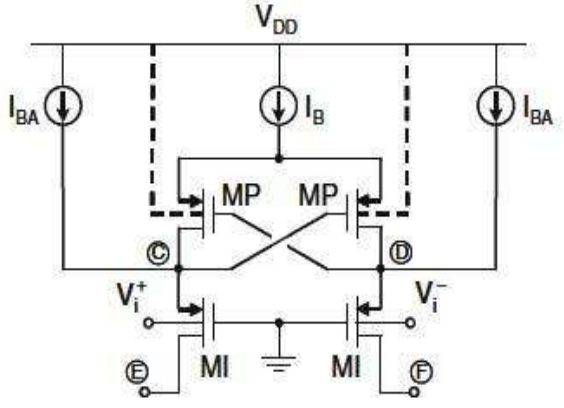

Fig. 3 Enhancement of transconductance by input differential pair

3. Bulk driven input stage with modified low voltage cascode biasing

Figure 2 proposed the first bulk driven input stage in the circuit, the transistor $ME_{A,B}$ and $MI_{A,B}$ consist of input stage core circuit. The operation of transistor $MI_{A,B}$ same as the conventional bulk driven PMOS differential pair shown in fig. 1(a). But the exception is that $ME_{B,A}$ crossed biased their gates.

The biasing circuitry which is formed by transistor $ME_{A,B}$, $MC_{1,2}$ and $MB_{1,2,3,4}$ is the modified version of topology which is based on EKV model [10]. In EKV model, source controls the forward current (I_F) whereas drain controls the reverse channel current (I_R). The onset saturation voltage ($V_{DS,\ SAT}$) can be expressed by using I_F and I_R [10] as

$$V_{DS,SAT} = 2U_T \log\left[\frac{e^{\sqrt{\frac{I_F}{(W/L)I_S}}}-1}{e^{\sqrt{\frac{I_R}{(W/L)I_R}}}-1}\right] \quad (5)$$

Where, $I_S = 2\mu_{cox}U_T^2/K$

U_T = Thermal voltage

By the above equation, when $I_F >> I_R$, irrespective of current flowing through the device, an onset $V_{DS,\ SAT}$ can be generated. The circuit shown in fig. 3, for transistor MC_2, the ratio for I_F and I_R can be expressed as

$$\frac{I_{F,MC_2}}{I_{R,MC_2}} = 1+\frac{m}{2}(1+2n) \quad (6)$$

Where n and m are equals to $(W/L)_{MB1} \big/ (W/L)_{MB2}$ and $(W/L)_{MC1} \big/ (W/L)_{MC2}$. By properly choosing the value on m and n, the value of the forward current can becomes much larger than the reverse current. Across drain to source of transistor MC_2, $V_{DS,SAT}$ can be expressed. Due to this the gate voltage of the transistors $ME_{A,B}$ can biased the gates of input pair $MI_{A,B}$.

The output of the crossed biased transistor ME_B and ME_A which forms auxiliary differential pair can modulate the gates of the $M1_{A,B}$. This configuration modulated the bulk and the gate terminal of $MI_{A,B}$ directly or indirectly by input signal. The effective transconductance can be expressed by

$$g_{m-in-eff} = 2 \times g_{mb,MI} \quad (7)$$

Where $g_{mb,MI}$ are bulk transconductance of transistor $MI_{A,B}$. As a result the effective transconductance at input stage is simply doubles regardless of the g_m and g_{mb} of the auxiliary differential pair.

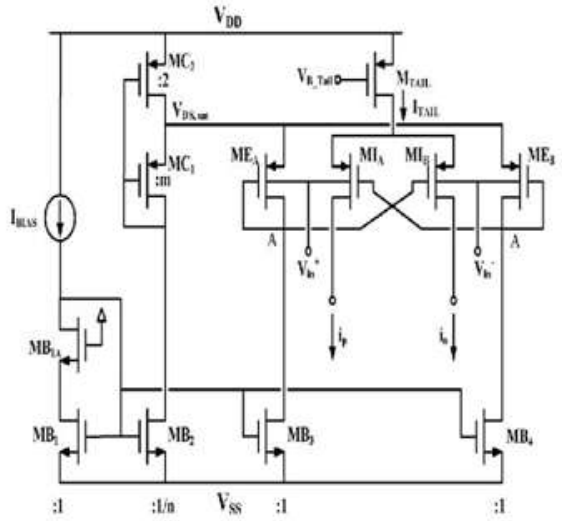

Fig. 4 Proposed input stage with modified cascode biasing scheme

4. Bulk driven input stage with effective enhance transconductance

To achieve more effective transconductance an improved version is proposed with a similar biasing scheme in figure 5. To improve the voltage gain from input to the gate of transistor, an additional auxiliary differential pair is used. As a result, transistor ME_{1B}, $ME_{2A}$and ME_{1A}, ME_{2B} from another cross biasing scheme, where both bulk and the gate of ME_{2A-B} are modulated to reduce the transistor count and to save power. The transconductance of ME_{1A-B} can be scaled $\boldsymbol{j}$ times smaller than that of ME_{2A-B}. The effective transconductance is thrice of $g_{mb,ME2}$. Transistor ME_{3A-B} which is a diode connected PMOS, there W/L ratio is scaled down to k times than the transistor ME_{2A-B} to increase the impedance at node A. Also the bulk or the gate transconductance ratio ($g_{mb,ME2A-B}$ /$g_{mb,ME3A-B}$ or $g_{m,ME2A-B}$ /$g_{m,ME3A-B}$) is equal to *k*.

By connecting the bulk terminal of ME_{3A-B} to the input signal the voltage gain get improved. If the output resistance of MOS device gets neglected then the total small signal voltage gain A_{aux} from the input to the node A can be expressed by

$$A_{aux} = 2 \times \frac{g_{mb,ME_2}}{g_{m,ME_3}} + \frac{g_{mb,ME_3}}{g_{m,ME_3}} \quad (8)$$

Including auxiliary voltage gain in previous equation, the effective transconductance can be derived as

$$g_{m-in-eff} = A_{aux} g_{m,MI} + g_{mb,MI} \quad (9)$$

Substituting $g_{mb,ME2}$ /$g_{mb,ME3}$ and $g_{m,ME2}$ /$g_{m,ME3}$ for parameter *k*, the simplified effective transconductance can be written as

$$g_{m-in-eff} = (2 \times k + 2) \times g_{mb,MI} \quad (10)$$

In the modified circuit the overall input transconductance doesn't depends on absolute g_{mb} or g_m values of auxiliary differential pairs without taking care of frequency dependent components. Compared with bulk driven stage proposed in section C, the circuit in figure 5 the circuit improves the effective trance conductance by $2 \times k$ times. But due to addition of few additional transistors at the input increases the current consumption.

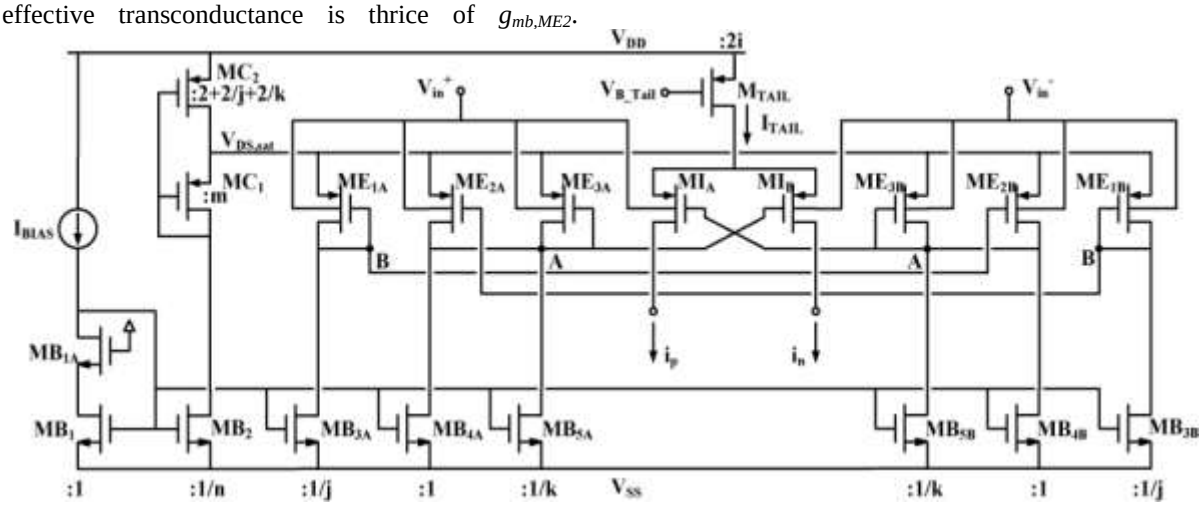

Fig. 5 Improved structure of modified cascade biasing

IV. NOISE

Due to low transconductance the noise immunity of bulk-driven is less than the immunity of gate-driven devices [1]. The partial positive feedback which is used in first two methods not only boost the signal of input devices but also noise current which is injected into the node where positive feedback action takes place. Due to partial positive feedback, the increase in the total output noise gets counteracted. The input referred noise also gets reduce by the increase in the DC gain. But in last two methods which is using auxiliary differential pairs, the problem of thermal noise and flicker noise arises. The thermal noise can be minimize by increasing the current consumption of auxiliary amplifier whereas

flicker noise can be treated by increasing the transistor sizing.

V. CONCLUSION

The effective transconductance of a bulk driven input stage amplifier can be increased by using the partial positive feedback approach or by using the auxiliary differential approach. Parameter like DC gain and GBW of the input stage also get increases due to the boosting of transconductance. Also the improvement in the noise can be treated by opting suitable measures in the above mention techniques.

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